ECE362 HW 8

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1. What are three operation modes of HC12 microcontrollers? And for each mode, specify the sizes of external address and data buses.

The 3 modes are single chip mode, expanded narrow mode, and expanded wide mode. The single chip mode has no external memory or I/O, while expanded narrow mode has external address and data buses enabled. Also, the expanded narrow mode has a 8-bit data interface used for external memory and I/O. Finally expanded wide mode has an external address and data buses enabled with a 16-bit data interface for external memory and I/O.

1. What kind of circuit do you need in order to extract address signals from a CPU with multiplexed address and data signals?

You use a simple latch, which is used for de-multiplexing the signal.

1. Why should a bidirectional buffer be used when connecting a CPU to the data bus?

This is necessary because data has to be sent and received through the data bus in order to properly read and write.

1. In the following circuit, there is an Optional Latch. Why is the Latch optional? In what situation is it essential and in what situation is it not necessary?

The latch is optional because it enables the possibility for 16-bit address values to be passed to the EPROM, otherwise only one latch would only allow for 8-bit address values. It’s necessary when 16-bit values are needed to be passed, however it is not necessary is 8-bit is sufficient.

1. Write paragraphs to explain the following 68HC12 timing diagram.
   1. Explain what the purpose of this diagram is

The purpose of this timing diagram is to precisely describe what is happening during system operation. It allows for us to understand what is occurring in the system at during a specific clock cycle. This diagram specifically gives us insight on a full clock signal and the passed addressed and data multiplexed values. Additionally, a timing diagram can be used to determine whether an address/data value is in a read/write state as that’ll enact a much different operation.

* 1. Explain who provides each signal at what time

The eclock signal is provided by the computer clock (by design), it’s a discrete time signal, so it is either on or off. This is indicated by 2 and 3 on the timing diagram given.

The read/write signal is given by a command to identify whether the data and address values should be read or written to the given address point. The address and data multiplexed values are also given on the lower portion of the timing diagram describing the operations that occur with read or write states within the system. This values for us to understand whether data is being written or read to a given address at a time in our system’s clock cycle. Finally, the DBE signal is used to indicate whether the multiplexed bus is used as the data bus.